REMARKS

This Amendment responds to the Notice of Non-Compliant Amendment dated December 3, 2003 in particularly to remove the single brackets and replace with strikethrough in compliance under the new revised practice.

This Amendment responds to the Office Action dated May 7, 2003 in which the Examiner rejected claims 7-9 and 16-18 under 35 U.S.C. §112, second paragraph, objected to the drawings, rejected claim 1 under 35 U.S.C. §102(b), rejected claims 2-18 under 35 U.S.C. §103 and objected to claims 19 and 20 as being dependent upon a rejected base claim but would be allowable if rewritten in independent form.

As indicated above, claims 7 and 16 have been amended in order to more particularly point out the additional feature of the ground conductor and to delete the microstripline. In addition, claims 8-9 and 17-18 were amended to more particularly point out the addition of a grounded coplanar line. It is respectfully submitted that the rejection to claims 7-9 and 16-18 no longer applies. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claims 7-9 and 16-18 under 35 U.S.C. §112, second paragraph.

In light of the amendments to claims 7-9 and 16-18, it is respectfully submitted that the objection to the drawings no longer applies. Therefore, it is respectfully requested that the Examiner withdraws the objection to the drawings.

Claim 1 claims a DC block circuit and claim 10 claims a communication equipment comprising a DC block circuit and first and second electric circuits. The DC block circuit comprises a conductive line, an interdigital capacitor and a chip capacitor. The conductive

line is disposed on one surface of a dielectric substrate. The interdigital capacitor is disposed on the one surface and forms a part of the conductive line. The chip capacitor is disposed so that the interdigital capacitor is sandwiched between the chip capacitor and dielectric substrate.

Through the structure of the claimed invention disposing the conductive line and interdigital capacitor on one surface of a dielectric substrate, as claimed in claims 1 and 10, the claimed invention provides an excellent reflection property and good transmission loss characteristic over a wide frequency band. Furthermore, since fluctuations in the distribution of an electromagnetic field which is generated in a microstripline can be suppressed, the generation of reflected waves is reduced by arranging an interdigital capacitor in contact with a chip capacitor. The prior art does not show, teach or suggest the invention as claimed in claims 1 and 10.

As indicated above, claims 1 and 10 have been amended to make explicit what is implicit in the claims. It is respectfully submitted that the amendment is unrelated to a statutory requirement for patentability and does not narrow the literal scope of the claims.

Claim 1 was rejected under 35 U.S.C. §102(b) as being anticipated by *Sugawara et al.* (U.S. Patent No. 5,636,099).

Sugawara et al. appears to disclose a variable capacitor used for a high frequency circuit of a high frequency apparatus, and more particularly to a variable capacitor formed by a multilayer circuit board. (Col. 1, lines 6-9) FIG. 2A is a plan view showing the first layer of a circuit board of a six-layer (L1 to L6) structure, FIG. 2B is a cross-sectional view of FIG. 2A, and FIG. 2C is a view showing a specific pattern of an interdigital capacitor formed at the

fourth layer. In FIGS. 2A to 2C, there are shown a chip capacitor 1, through holes 2 to 5 respectively connected to interdigital capacitors of the second to fifth layer, a wiring pattern 6 for soldering the chip capacitor 1, interdigital capacitors 7 to 10 formed at the second to fifth layers, respectively. The capacitor 7 is connected to the through hole 2, the capacitor 8 is connected to the through hole 3, the capacitor 9 is connected to the through hole 4 and the capacitor 10 is connected to the through-hole 5, respectively. These interdigital capacitors 7 to 10 are previously set so as to have a different capacity, respectively. Capacitance select portions A are formed on the wiring pattern 6 for causing disconnection between the through hole 3 and the capacitor 8. (Col. 2, lines 20-37)

Thus, *Sugawara et al.* merely discloses a wiring pattern 6 formed on a top layer and interdigital capacitors 7-10 formed on second to fifth layers respectively. Thus nothing in *Sugawara et al.* shows, teaches or suggests both the conductive line and interdigital capacitor are disposed on one surface of a dielectric substrate as claimed in claim 1. Rather, *Sugawara et al.* teaches away from the claimed invention since the interdigital capacitors 7-10 are disposed on different layers then the wiring pattern 6.

Since nothing in *Sugawara et al.* shows, teaches or suggests an interdigital capacitor and conductive line disposed on one surface of a dielectric substrate as claimed in claim 1, it is respectfully requested that the Examiner withdraws the rejection to claim 1 under 35 U.S.C. §102(b).

Claims 2-9 were rejected under 35 U.S.C. §103 as being unpatentable over *Sugawara et al.*

Applications respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, it is respectfully requested that the Examiner withdraws the rejection to the claims allows the claims to issue.

As discussed above, since nothing in *Sugawara et al.* shows, teaches or suggests disposing a conductive line and an interdigital capacitor on one surface of the dielectric substrate as claimed in claim 1, it is respectfully submitted that the rejection to claims 2-9 no longer applies. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claims 2-9 under 35 U.S.C. §103.

Claims 10-18 were rejected under 35 U.S.C. §103 as being unpatentable over *Lau* (U.S. Patent No. 5,896,417) in view of *Sugawara et al.*.

Lau appears to disclose 10Base-T receiver 32R and 100Base-TX receiver 42R have different DC input bias levels. To avoid DC input discrepancy between receivers 32R and 42R, incoming signals RXH± are AC coupled to receiver 32R. In particular, conductors 70+ and 70- are tapped at nodes D+ and D- from where they are coupled through equal-value DC blocking capacitors CR+ and CR- to a pair of data input terminals, referred to as the RXI1+ and RXIL- terminals, of receiver 32R. Capacitors CR+ and CR- respectively block any DC components present in signals RXH+ and RXH- to produce differential incoming data signals RXI1+ and RXIL- at the RXI1+ and RXIL- terminals. (Col. 12, lines 55-66)

Thus, *Lau* merely discloses communication equipment including a block capacitor. Nothing in *Lau* shows, teaches or suggests the structure of the block circuit as claimed in claim 10.

As discussed above *Sugawara et al.* merely discloses interdigital capacitors 7-10 disposed on different layers from the wiring pattern 6. Thus nothing in *Sugawara et al.* shows, teaches or suggests disposing a conductive line and an interdigital capacitor on one surface of the dielectric substrate as claimed in claim 10.

The combination of *Lau* and *Sugawara et al.* would merely suggest to replace the block circuits of *Lau* with the block structure of Sugawara et al.. Thus nothing in the combination of the references shows, teaches or suggests disposing the interdigital capacitor and conductive line on one surface of the dielectric substrate as claimed in claim 10. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claim 10 under 35 U.S.C. §103.

Claims 11-18 depend from claim 10 and recite additional features. It is respectfully submitted that claims 11-18 would not have been obvious within the meaning of 35 U.S.C. §103 over *Lau* and *Sugawara et al.* at least for the reasons as set forth above. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claims 11-18 under 35 U.S.C. §103.

Since objected to claims 19 and 20 depend from allowable claims, it is respectfully requested that the Examiner withdraws the objection thereto.

The prior art of record, which is not relied upon, is acknowledge. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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